Remarks

This is in response to the non-final Office Action mailed on August 12, 2004. Claims 1 and 6 have been amended, and claims 1-6 remain pending. Reconsideration and allowance are respectfully requested in view of the following remarks.

Claims 1, 2, 4, and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kinoshita, U.S. Patent No. 5,869,852, in view of Miki, U.S. Patent No. 5,761,076. This rejection is respectfully traversed, to the extent it is maintained.

Claim 1 recites (i) that a capacitance value of the power supply capacitor cell is determined based on a drive load capacity value of a logic gate cell, and (ii) arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value of the power supply capacitor cell.

Therefore, claim 1 recites that the power supply capacitor cell is arranged, not in the vicinity of any logic gate cell, but rather in the vicinity of the logic gate cell that is used to determine the capacitance value of the power supply capacitor cell. Such a configuration is advantageous because noise created by the power supply can be suppressed.

The rejection concedes that Kinoshita fails to disclose or suggest that a capacitance value of the power supply capacitor cell is determined using a drive load capacity value of the logic gate cell, as recited by claim 1. In addition, Kinoshita fails to suggest the power supply capacitor being arranged in a vicinity of a logic gate cell that is used to determine the capacitance value of the power supply capacitor cell, as recited by claim 1.

Miki discloses a method in which a capacitance of wirings is calculated to determine a delay time. See Miki, col. 1, ll. 20-32. However, Miki does not disclose or suggest that a capacitance value of a power supply capacitor cell is determined based on a drive load capacity value of a logic gate cell, as recited by claim 1. In addition, Miki fails to suggest the power supply capacitor being arranged in a vicinity of a logic gate cell that is used to determine the capacitance value of the power supply capacitor cell, as recited by claim 1

For at least these reasons, neither Kinoshita nor Miki, alone or in combination, discloses or suggests an LSI layout method as recited by claim 1. Reconsideration and allowance of claim 1, as well as claims 2 and 4 that depend therefrom, are respectfully requested.

Claim 6 is similar to claim 1, except that claim 6 recites that the power supply capacitor cell is arranged adjacent to the logic gate cell. For similar reasons to those noted above with

respect to claim 1, neither Kinoshita nor Miki renders claim 6 obvious under section 103(a). Reconsideration and allowance are respectfully requested.

Claim 5 was rejected under section 103(a) as being unpatentable over Kinoshita in view of Miki and further in view of Kusunoki et al., U.S. Patent No. 5,512,766. In addition, claim 3 was rejected under section 103(a) as being unpatentable over Kinoshita in view of Miki and further in view of Eto et al., U.S. Patent No. 6,229,363. These rejections are respectfully traversed, and the correctness of the rejections is not conceded.

However, neither Kusunoki nor Eto remedies the shortcomings of Kinoshita and Miki noted above with respect to claim 1. Claims 3 and 5 depend from claim 1. Therefore, claims 3 and 5 should be allowable for at least the same reasons as claim 1. Reconsideration and allowance are respectfully requested.

In view of the above supplemental remarks, favorable reconsideration of claims 1-6 in the form of a Notice of Allowance is requested. The Examiner is invited to contact the undersigned at (612) 371-5237 with any questions regarding this application.

Respectfully submitted,
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